Claims

We claim the following invention:

1. A System-on-Chip (SOC) apparatus having a latency-tolerant architecture, comprising:

a processor core;

one or more peripherals; and

a first internal bus that couples said processor core to said peripheral(s) and carries signals from signal initiators to signal targets, said first internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target.

2. The System-on-Chip (SOC) apparatus of claim 1 wherein said one or more peripherals further comprises one or more DMA-type peripherals, and said apparatus further comprises:

a memory subsystem; and

a second internal bus that couples said processor core to said memory subsystem and to said DMA-type peripherals, said second internal bus carries signals from signal initiators to signal targets, said second internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target.

3. The System-on-Chip (SOC) apparatus of claim 1 or claim 2, wherein said signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking.

4. The System-on-Chip (SOC) apparatus of claim 1 or claim 2, wherein said pipeline stages further comprise one or more of the following: flip-flop, multiplexing router, or decoding router.

5. The System-on-Chip (SOC) apparatus of claim 2, wherein said first internal bus and said second internal bus have overlapping topologies, each topology further comprising one or more of the following topologies: matrix fabric (or woven) topology, point-to-point topology, bridged topology, or bussed topology.

6. A System-on-Chip (SOC) system having a latency-tolerant architecture, comprising:

a processor core;

one or more peripherals; and

a first internal bus that couples said processor core to said peripheral(s) and carries signals from signal initiators to signal targets, said first internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target.

7. The System-on-Chip (SOC) system of claim 6 wherein said one or more peripherals further comprises one or more DMA-type peripherals, and said system further comprises:

a memory subsystem; and

a second internal bus that couples said processor core to said memory subsystem and to said DMA-type peripherals, said second internal bus carries signals from signal initiators to signal targets, said second internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any

signal target.

8. The System-on-Chip (SOC) system of claim 6 or claim 7, wherein said signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking.

9. The System-on-Chip (SOC) system of claim 6 or claim 7, wherein said pipeline stages further comprise one or more of the following: flip-flop, multiplexing router, or decoding router.

10. The System-on-Chip (SOC) system of claim 7, wherein said first internal bus and said second internal bus have overlapping topologies, each topology further comprising one or more of the following topologies: matrix fabric (or woven) topology, point-to-point topology, bridged topology, or bussed topology.

11. A method to manufacture a System-on-Chip (SOC) apparatus having a latency-tolerant architecture, comprising:

providing a processor core;

providing one or more peripherals; and

coupling a first internal bus to said processor core and to said peripheral(s), said first internal bus carries signals from signal initiators to signal targets, said first internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target.

12. The method of claim 11 wherein said one or more peripherals further comprises one or more DMA-type peripherals, and said method further comprises:

providing a memory subsystem; and

coupling a second internal bus to said processor core, to said memory subsystem, and to said DMA-type peripherals, said second internal bus carries signals from signal initiators to signal targets, said second internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target.

13. The method of claim 11 or claim 12, wherein said signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking.

14. The method of claim 11 or claim 12, wherein said pipeline stages further comprise one or more of the following: flip-flop, multiplexing router, or decoding router.

15. The method of claim 12, wherein said first internal bus and said second internal bus have overlapping topologies, each topology further comprising one or more of the following topologies: matrix fabric (or woven) topology, point-to-point topology, bridged topology, or bussed topology.

16. A method of using a System-on-Chip (SOC) apparatus having a latency-tolerant architecture, comprising:

providing a processor core;

providing one or more peripherals; and

carrying signals from signal initiators to signal targets over a first internal bus that couples said processor core to said peripheral(s), said first internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target.

17. The method of claim 16 wherein said one or more peripherals further comprises one or more DMA-type peripherals, and said method further comprises:

providing a memory subsystem; and

carrying signals from signal initiators to signal targets over a second internal bus that couples said processor core to said memory subsystem and to said DMA-type peripherals, said second internal bus has a latency tolerant signal protocol that allows an arbitrary number of pipeline stages between any signal initiator and any signal target.

18. The method of claim 16 or claim 17, wherein said signals are point-to-point and registered signals, and said latency tolerant signal protocol further comprises full handshaking.

19. The method of claim 16 or claim 17, wherein said pipeline stages further comprise one or more of the following: flip-flop, multiplexing router, or decoding router.

20. The method of claim 17, wherein said first internal bus and said second internal bus have overlapping topologies, each topology further comprising one or more of the following topologies: matrix fabric (or woven) topology, point-to-point topology, bridged topology, or bussed topology.